IN THE SPECIFICATION:

Please amend the specification pursuant to 37 C.F.R. §1.121 as follows (see the accompanying "marked-up" version pursuant to §1.121):

On page 4, delete the third paragraph, and insert the following:

Logic gates configured in accordance with the present invention are less sensitive to transistor collector capacitance and/or wiring capacitance on the collectors of the transistors T3, T4, T5, T6. In addition, the topology shown in Figure 3a provides a convenient node in the circuit that can be used for input/output connections between logic gates. Specifically, logic gates in accordance with the present invention are arranged to have a TIS input stage and a TAS output stage. Here, element 305 is an exemplary TIS block or latch that is configured in accordance with the present invention. Thus, the current from the switched TAS output is received by the TIS input stage of the next logic block in the cascaded logic chain. A TIS block or latch is also shown in the incorporated U.S. Patent No. 6,297,706, e.g., see element 24 of Figs. 2 and 3. See also, the description at: col. 2, lines 46-54.

IN THE CLAIMS:

Please amend the claims pursuant to 37 C.F.R. §1.121 as follows (see the accompanying "marked-up" version pursuant to §1.121):

8. (Amended) The cascaded latch chain in accordance with claim 7, further comprising at least one latch pair connected to receive the output current of said clocked trans-admittance